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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,902	08/02/2001	Masahiko Watanabe	35.C15650	4530

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EXAMINER
NGUYEN, LAM S

ART UNIT	PAPER NUMBER
2853	

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/919,902	WATANABE, MASAHIKO	
	Examiner	Art Unit	
	LAM S NGUYEN	2853	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4, 7/1-4, 8/1-4, 9/7/1-4, and 10/1-6, 11/7/1-6, 12/8/1-6, 13/9/7/1-6 ,,14, 17 is/are rejected.

7)☒ Claim(s) 5, 6, 7/5-6, 8/5-6, 9/7/5-6, 10/5-6, 15, 16 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02 August 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

The substitute specification filed on April 11, 2002 is accepted since it contains no new matter and includes a marked-up copy.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

1. Claims 1-4, 7/1-4, and 17 are rejected under 35 U.S.C. 102(a) as being obvious by Hoshino (JP 2001-100873).

Hoshino discloses an integrated-circuit apparatus comprising:

a CPU (FIG. 1, element 8); and

a plurality of circuit blocks (FIG. 2, element 31-3n) to be initialized in accordance with external reset signals (in term of "initial configuration start signal") (FIG. 1, element 1c: signal 1c is external of the circuit blocks), wherein

the circuit blocks each respectively output an initialization completion signal (in term of "initialization success signal") (FIG. 2, elements 31g-31ng) for communicating completion of initialization after the circuit blocks are initialized , and

the CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks (FIG. 3a, element 3: After the CPU receives the setting terminate signal 1e that is in accordance

to the initialization success/failure signal 1d, the firmware inside the CPU performs processing which confirms whether it can operate normally to each circuit block (in term of "a line card block" (paragraphs 17 and 18). Therefore, it is inherent that there exists a signal such as an enable signal generated by the C

PU after the CPU receives the setting terminate signal 1e).

Referring to claim 2: wherein the circuit blocks are initialized to output the initialization completion signals (FIG. 2, element 31g-31ng), and said apparatus further comprises a logic circuit (FIG. 2, element 4) for inputting the initialization completion signals (FIG. 2, element 3g) output from the circuit blocks to logic-operate the signals, and outputting the logic-operation results (FIG. 2, element 1e) to the CPU (FIG.1, element 8).

Referring to claims 3, 4: wherein when all of the circuit blocks are initialized, the CPU outputs the enable signal to all the circuit blocks (FIG. 2, element 4: when all the initialization completion signals (FIG. 2, element 3g) are inputted into the AND gate via the element 3g in the element 4, the signal 1e is generated. Then, after the CPU receives the setting terminate signal 1e in accordance to the initialization success/failure signal 1d, the firmware inside the CPU performs processing which confirms whether it can operate normally to each circuit block. As expressed above, the CPU generates a signal such as an enable signal, inherently).

Referring to claim 7/1-4: wherein the circuit blocks output the initialization completion signals when a predetermined period passes after the reset signal is input (paragraph 6: teaching a setup time of the initial configuration).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 8/1-4, 9/7/1-4, and 10/1-4, 11/7/1-4, 12/8/1-4, 13/9/7/1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshino (JP 2001-100873) in view of Mitani (US 5929672).

Hoshino discloses the claimed invention as discussed above except wherein the integrated-circuit apparatus is constituted of one chip.

However, Mitani discloses a power on reset circuit including a CPU and the circuit blocks (FIG. 4) that is constituted of one chip (column 5, line 23-26).

Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to constitute the CPU and the circuit blocks as disclosed by Hoshino in a chip as taught by Mitani because the one-chip configuration decreases time for the signal propagation in order to increase the speed of the data processing.

Referring to claims 10/1-4, 11/7/1-4, 12/8/1-4, 13/9/7/1-4: it is noted that the intended use of the claimed invention is not given patentable weight because the limitation teaching the use of this apparatus in a printer does not depend on the preamble for completeness (See MPEP 2111.02).

3. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nitta et al. (US 5784080) in view of Hoshino (JP 2001-100873).

Nitta et al. discloses an ink-jet recording apparatus (column 1, line 17) comprising:

an integrated-circuit apparatus for controlling recording (FIG. 4) using a recording head , wherein the integrated-circuit apparatus comprises:

a CPU (FIG. 4, element 55); and

a plurality of circuit blocks (FIG. 4, elements 57, 59)

a control circuit (FIG. 4)

a driving circuit (FIG. 4, element 53)

Nitta et al. does not disclose that circuit blocks are initialized in accordance with external reset signals, the circuit blocks each respectively output an initialization completion signal for communicating completion of initialization after the circuit blocks are initialized, and the CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks.

However, Hoshino discloses the circuit blocks are initialized in accordance with external reset signals (FIG. 1, element 1c), the circuit blocks each respectively output an initialization completion signal (FIG. 2, element 31g-3ng) for communicating completion of initialization after the circuit blocks are initialized, and the CPU (FIG. 1, element 8) outputs an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks (FIG. 3a, element 3: After the CPU receives the setting terminate signal 1e that is in accordance to the initialization success/failure signal 1d, the firmware inside the CPU performs processing which confirms whether it can operate normally to each circuit block (in term of "a line card block" (paragraphs 17 and 18). Therefore, it is inherent

that there exists a signal such as an enable signal generated by the CPU after the CPU receives the setting terminate signal 1e).

Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to include such initialization process as designed by Hoshino into the design of Nitta et al. because this process makes sure the circuit blocks are configured completely before starting their operations in order to avoid the unstable operations caused by the failure initialization process.

Allowable Subject Matter

4. Claims 5, 6, 7/5-6, 8/5-6, 9/7/5-6, 10/5-6, 15, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Referring to claims 5, 6, 7/5-6, 8/5-6, 9/7/5-6, 10/5-6: The limitation teaching wherein if there is any circuit block that is not initialized yet, the CPU initializes the circuit block by using the enable signal is not disclosed in the prior art.

Referring to claims 15 and 16: The limitations teaching the circuit blocks each respectively output a signal for initializing the control circuit, and the circuit blocks each respectively output a signal for initializing the driving circuit are not disclosed in the prior arts.

Response to Arguments

Applicant's arguments filed 04/11/2002 have been fully considered but they are not persuasive.

Referring to the argument regarding to claims 1, 14, and 17 on page 9: The applicant argues that Hoshino fails to disclose the CPU outputting an enable signal for permitting

operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks. However, as discussed above, Hoshino discloses the CPU outputting an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks. Therefore, the Hoshino reference overcomes the argument of the applicant. As a result, the claims 1, 14, and 17 are unpatentable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAM S NGUYEN whose telephone number is (703)305-3342. The examiner can normally be reached on 7:00AM - 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JOHN E BARLOW can be reached on (703)308-3126. The fax phone numbers for the organization where this application or proceeding is assigned are (703)305-3431 for regular communications and (703)305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

LN

July 15, 2002

John Barlow
Supervisory Patent Examiner
Technology Center 2800